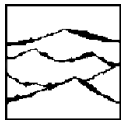

WAVECREST Corporation

Testing 100BaseT Devices Utilizing Low-cost ATE and the WAVECREST TEM75+

Application Note No. 135

200135-00 REV A

WAVECREST Corporation continually engages in research related to product improvement. New material, production methods, and design refinements are introduced into existing products without notice as a routine expression of that philosophy. For this reason, any current *WAVECREST* product may differ in some respect from its published description but will always equal or exceed the original design specifications unless otherwise stated.

WAVECREST Corporation
A Technologies Company
7626 Golden Triangle Drive
Eden Prairie, Minnesota 55344
(952) 831-0030
(800) 733-7128
www.wavecrest.com

First Printing: January 2002

U.S. Patent Nos. 4,908,784 and 6,185,509 and 6,194,925; other United States and foreign patents pending

This page intentionally left blank.

Contents

This page intentionally left blank.

Testing 100BaseT Devices Utilizing Low-cost ATE and the WAVECREST TEM75+

Application Note 135

INTRODUCTION

A high-speed communication device (100BaseT) can be compliance tested at comparable speeds on less-expensive (<$500K) ATE with the addition of peripheral instrumentation ($100K), thus reducing cost-of-test/part.

The challenges of testing LAN devices on ATE include synchronizing external data generators with the ATE drive/receive pins and the free-running clock pin, designing low-jitter synchronous triggers on the DUT board, establishing a library of signals to be used in receive testing that replicate the distortion induced by differing lengths of cable and looping on vector patterns while controlling external instrumentation.

The physical layer 100BaseT device communicates either directly through a Media Independent Interface (MII) or through a Media Access Controller (MAC) at parallel speeds of 25MHz, which are converted to or derived from a 125MHz serial data stream. The only high-speed device pins are the differential transmit and receive, which are analog multi-level (3) transformations (MLT-3) of the serial data stream. Therefore, with proper instrumentation connected to receive and transmit ports, plus the proper synchronization circuitry, a lower-speed and lower-cost tester can be used to send and compare the digital data. For this setup, Credence SC series ATE and the Wavecrest TEM75+, incorporating a high-speed (>= 1Gs/s) AWG with a Wavecrest DTS-2075, were used. Two capabilities of the Wavecrest 2075 were utilized, oscilloscope mode and histogram mode, to measure and analyze the transmit signal of the device.

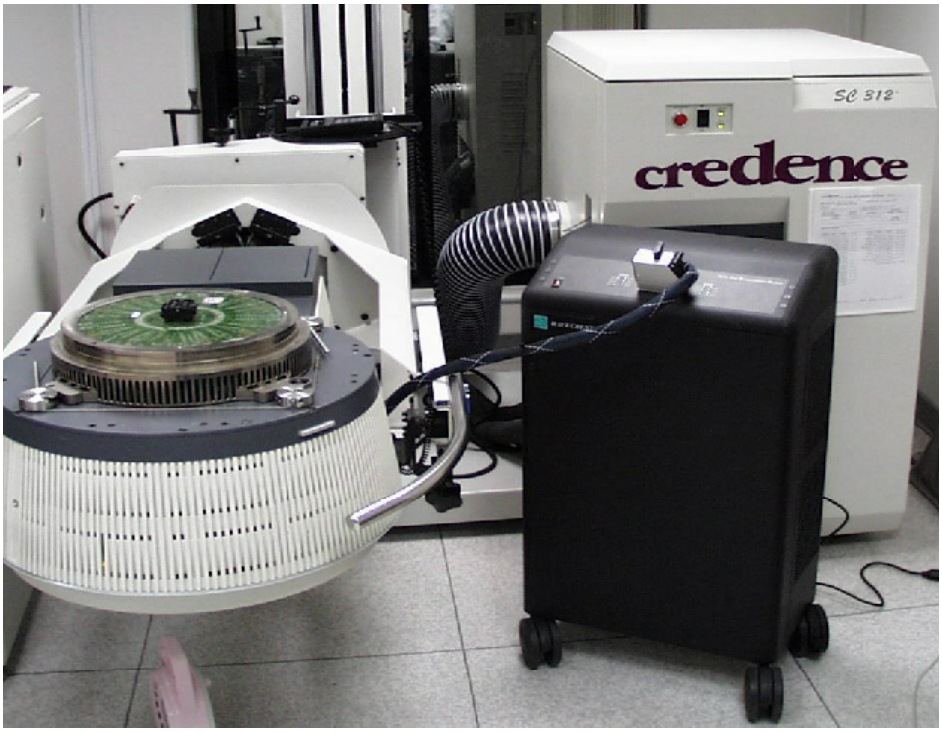

Figure 1 - Credence SC312 and *WAVECREST* TEM75+

The device being tested is the Intel LXT970A Dual-Speed Fast Ethernet Transceiver. It has the capabilities of operating in either 10BaseT or 100BaseT mode and can transmit and receive on either copper (TX mode) or optical fiber (FX mode). This device is a physical layer device without an embedded MAC. For this test program, only the 100BaseT copper interface is tested, although the DUT board design is set up to enable testing of all modes.

GENERAL TRANSMIT TEST SETUP

The device is programmed to output an MLT-3 idle waveform with a short burst of data as illustrated. The idle waveform portion has 8ns between each voltage transition and the data waveform portion has 16ns between each voltage transition. The upper trace is the transmit output and the lower trace is a reference trigger signal. To make an accurate waveform measurement, the trigger signal must be gated, synchronous to the edges of the measured waveform, and have very low added jitter, less than the resolution of sampling, otherwise the rising and falling edges will appear to have added noise on them due to the output dispersion of the trigger circuitry.

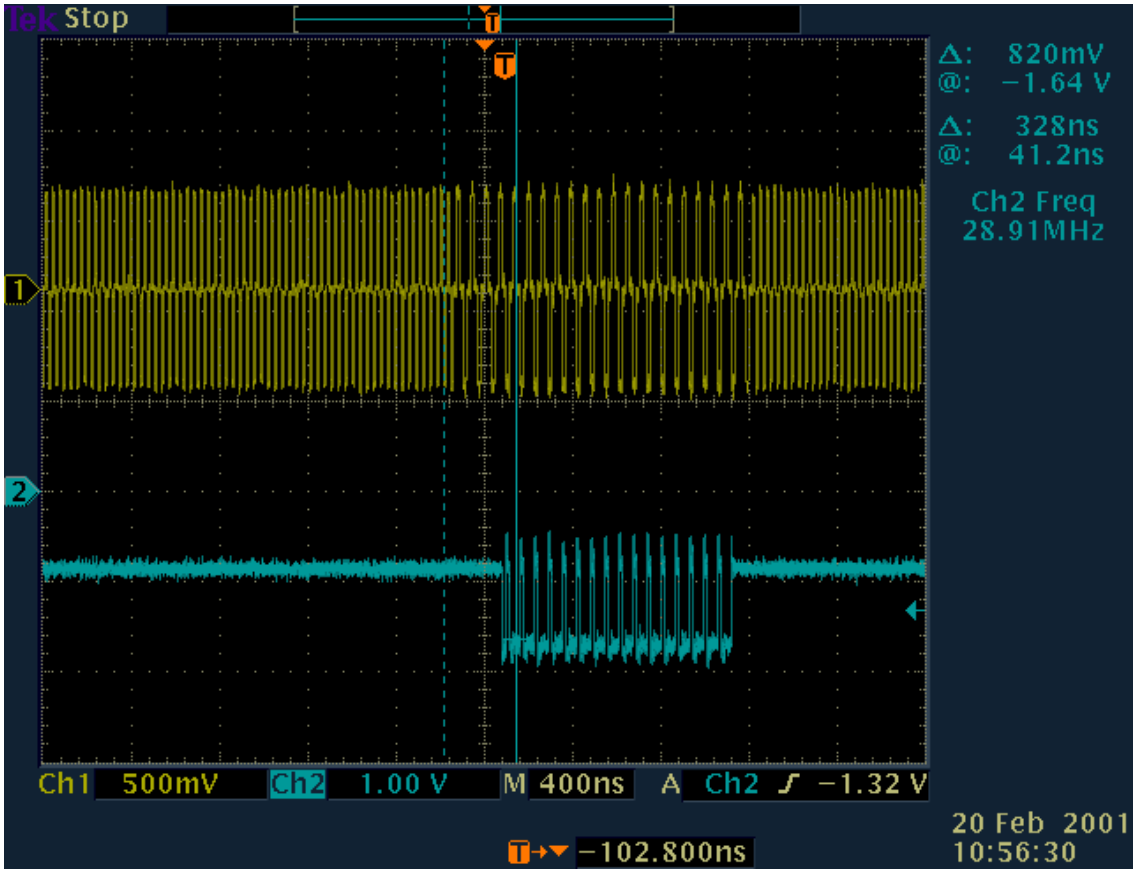

Figure 2 - MLT-3 Idle Waveform, Data Waveform, and Trigger

The next illustration is an expanded view of the waveforms during the data transmission.

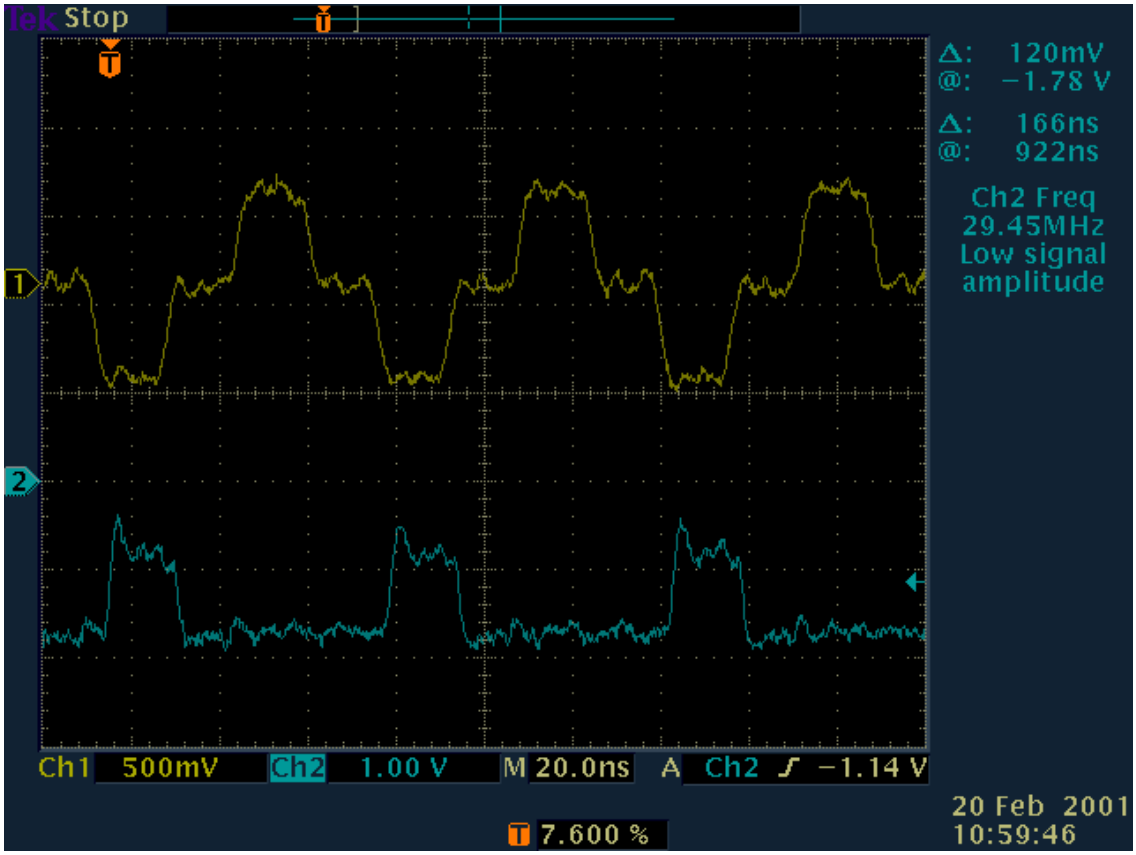

Figure 3 MLT-3 Data Waveform and Trigger, Expanded View

To sample the waveform, the *WAVECREST* DTS-2075 digitizes one complete cycle of the MLT-3 waveform, at 50ps and 150uV resolution, using the trigger signal as a time reference. This results in a 64ns waveform with 1280 data points. Because the *WAVECREST* DTS-2075 is a comparator-based measurement tool, a successive-approximation technique is used to acquire the sample voltages. The resulting waveform is then analyzed to determine the characteristics of high and low levels, mid-level, overshoot and undershoot, rise and fall times, and duty-cycle distortion.

The *WAVECREST* DTS-2075 then asynchronously measures multiple periods of the MLT-3 data signal to capture all jitter components and calculates peak-to-peak jitter.

GENERAL RECEIVE TEST SETUP

The AWG is programmed to output a composite signal to test three receive test parameters simultaneously: Adaptive Equalization, Baseline Wander Correction and Jitter Tolerance. The following illustration shows two traces: 1) a zero cable length pseudorandom bit stream that translates to a repeating 5-bit 32-vector digital pattern; and 2) the corresponding waveform at the end of a 100 meter CAT-5 cable, with jitter and baseline wander added. For this particular waveform, the attenuation is MLT-3 data level time dependent, the baseline is offset by as much as 250mV, and the jitter at a level transition of 100mV is approximately 4ns.

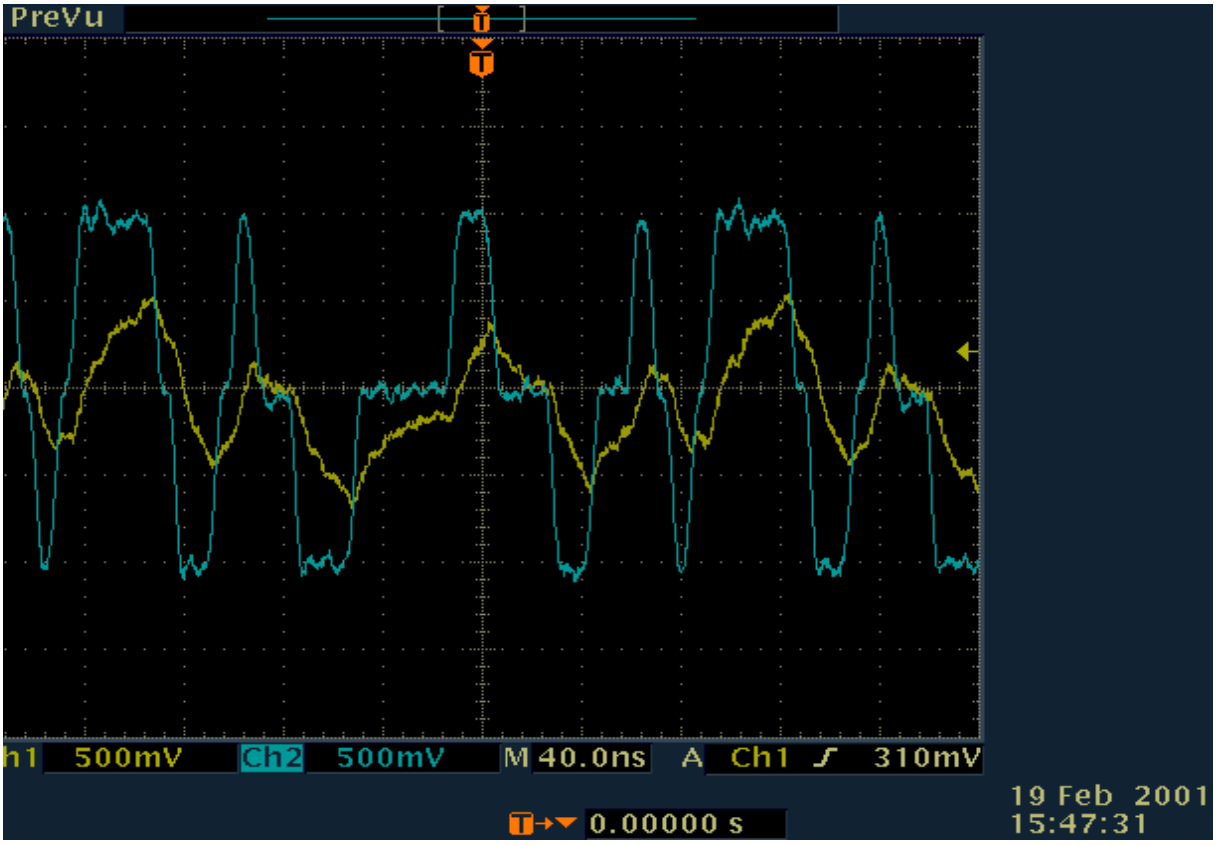

Figure 4 - MLT-3 PRBS Data Waveforms, CAT-5 cable: 0 meter (blue) and 100 meter (yellow)

The digital pattern is sampled and compared by the ATE to verify proper data translation. To enable the ATE to sample the data at proper times, the AWG is synchronized to the device clock by additional DUT board circuitry and triggered by the ATE.

RESULTS

As a result of marketing research and consultation with potential customers, acceptable test time was determined to be:

Receive tests, excluding jitter	1500ms
Jitter measurement	500ms
Receive parameters testing	1000ms
Total	3000ms

Actual test times are:

Waveform sampling	250ms
Waveform characteristic analysis	150ms
Jitter measurement	120ms
Receive parameters testing	120ms
Total	640ms

CONCLUSION

Testing costs of high-speed communication devices can be significantly reduced by changing test platforms to less expensive ATE and the addition of specific peripheral instrumentation. In addition, product engineers can use the extensive graphical analysis tools in the *WAVECREST* TEM75+, with the same test hardware, to determine sources of failure that cause production yield shifts.

This page intentionally left blank.

WAVECREST Corporation

World Headquarters:
7626 Golden Triangle Drive
Eden Prairie, MN 55344
(952) 831-0030
FAX: (952) 831-4474
Toll Free: 1-800-733-7128
www.wavecrest.com

West Coast Office:
1735 Technology Drive, Ste. 400
San Jose, CA 95110
(408) 436-9000
FAX: (408) 436-9001
1-800-821-2272

Europe Office:
Lilenthalalle 25
D-80939 Munchen
011-49-89-32225330
FAX: 011-49-89-32225333

Japan Office:
2-1 Ohtemachi 2-Chome
Chyoda-Ku, Tokyo 100-0004, Japan
81-3-5960-5770

200135-00 REV A